AMENDMENTS TO THE CLAIMS

1. (Original) An integrated circuit (IC) having programmable interconnections, comprising:

a first plurality of regions, each region having a programmable circuit with a programmable function; and

a second plurality of column-like areas of the IC, wherein each column-like area of the second plurality extends from one edge of the IC to an opposing edge of the IC, and wherein each column-like area of the second plurality comprises predetermined regions of the first plurality, wherein the predetermined regions in a column-like area substantially fill the column-like area and wherein each of the predetermined regions in the column-like area comprises programmable circuits substantially identical to programmable circuits in at least two other predetermined regions in the column-like area.

2. (Currently Amended) The integrated circuit of claim 1 wherein ~~each~~ every predetermined region in the predetermined regions in the column-like area has a circuit of only one circuit type, the circuit type selected from a group consisting of Configurable Logic Block (CLBs), Multi-Giga Bit Transceivers (MGTs), Block Random Access ~~Memory~~ Memories (BRAMs), Digital Signal Processor (DSP) circuits, Multipliers, and Input/Output ~~Buffer~~ Blocks (IOBs).

3. (Original) The integrated circuit of claim 1 wherein a column-like area of the second plurality has predetermined regions comprising Multi-Giga Bit Transceiver (MGT) circuits.

4. (Currently Amended) The integrated circuit of claim 1 further comprising a heterogeneous column-like area of the IC, the heterogeneous column-like area having regions with programmable circuits that are of different circuit types.

5. (Original) A die having an integrated circuit, comprising:

a first set of regions, each region in the first set having an Input/Output circuit;

a second set of regions, each region in the second set having a circuit with a programmable logic function;

a third set of columns, wherein a top of each column of the third set is positioned at a top side of the die and a bottom of each column of the third set is positioned at a bottom side of the die;

a first column of the third set consisting essentially of regions from the first set; and

a second column of the third set consisting essentially of regions from the second set, wherein the second column is interposed between the first column and a nearest side edge of the die.

6. (Currently Amended) The die of claim 5 wherein an Input/Output circuit comprises a Multi-Giga Bit Transceiver ~~MGT circuit~~ or ~~a IOB~~ an input/output block ~~circuit~~ or a combination thereof.

7. (Original) The die of claim 5 further comprising a third column of the third set positioned at a center line of the die, the third set comprising assorted tiles.

8. (Original) An integrated circuit disposed on a semiconductor die, wherein the integrated circuit comprises a plurality of columns, each of the columns is completely occupied by a plurality of tiles, wherein substantially all of the tiles of each of the columns have an identical width, wherein a width of one of the columns differs from a width of another of the columns, and wherein there are input/output block tiles disposed in at least two of the columns.

9. (Original) The integrated circuit of Claim 8, wherein the semiconductor die has a first side, a second side parallel to the first side, a third side, and a fourth side parallel to the third side, and wherein each column of the plurality of columns extends from the first side to the second side.

10. (Original) The integrated circuit of Claim 8, wherein the semiconductor die has a first side, a second side parallel to the first side, a third side, and a fourth side parallel to the third side, and wherein one of the columns is a column of configurable logic block tiles, the column of configurable logic block tiles extending from the first side to the second side such that a first configurable logic block tile is disposed adjacent the first side and such that a second configurable logic block tile is disposed adjacent the second side.

11. (Original) The integrated circuit of Claim 10, wherein all the configurable logic block tiles of the column of configurable logic block tiles are identical tiles.

12. (Original) The integrated circuit of Claim 10, wherein there is no input/output block tile disposed between the column of configurable logic block tiles and the first side of the semiconductor die, and wherein there is no input/output block tile disposed between the column of configurable logic block tiles and the second side of the semiconductor die.

13. (Original) The integrated circuit of Claim 8, wherein each of the input/output block tiles is coupled by a conductor to an associated bond bump, and wherein circuitry of the input/output block tile can be configured to use the bond bump to receive a signal onto the integrated circuit via the input/output block tile.

14. (Original) The integrated circuit of Claim 8, wherein the semiconductor die has a first side, a second side parallel

to the first side, a third side, and a fourth side parallel to the third side, and wherein at least one of the columns is a column of input/output block tiles, the column of input/output block tiles extending from the first side to the second side such that an input/output block tile is disposed adjacent the first side and such that a second input/output block tile is disposed adjacent the second side.

15. (Original) The integrated circuit of Claim 14, wherein all the input/output block tiles of the column of input/output block tiles are identical tiles.

16. (Original) The integrated circuit of Claim 8, wherein one of the columns includes at least four different types of tiles.

17. (Original) The integrated circuit of Claim 8, wherein a column of the plurality of columns includes a plurality of clock distribution tiles.

18. (Original) The integrated circuit of Claim 8, wherein over ninety-five percent of the die area of each of the columns is occupied by a single type of tile.

19. (Original) The integrated circuit of Claim 18, wherein in addition to the single type of tile each of the columns also includes a plurality of clock distribution tiles.

20. (Original) The integrated circuit of Claim 8, wherein substantially all the input/output block tiles are laid out to have either a first orientation or a second orientation, where the second orientation is a mirror image of the first orientation.

21. (Original) A method, comprising:
providing a plurality of configurable logic blocks in a

column, the column extending from a first side of an integrated circuit die to a second side of the integrated circuit die.

22. (Original) The method of Claim 21, further comprising:

providing a first input/output block on a first side of the column; and

providing a second input/output block on a second side of the column.

23. (Original) The method of Claim 22, wherein there is no input/output block disposed between the column of configurable logic blocks and the first side of the integrated circuit die, and wherein there is no input/output block disposed between the column of configurable logic blocks and the second side of the integrated circuit die.

24. (Original) The method of Claim 21, wherein the column includes the plurality of configurable logic blocks as well as a plurality of clock distribution tiles.

25. (Original) The method of Claim 21, wherein over ninety-five percent of the die area of the column is occupied by configurable logic blocks.

26. (Original) An integrated circuit, comprising:

a column of tiles including input/output block tiles, wherein the column of tiles occupies a die area, and wherein over ninety-five percent of the die area of the column is occupied by input/output block tiles;

a first configurable logic block tile disposed on a first side of the column; and

a second configurable logic block tile disposed on a second side of the column opposite the first side.

27. (Original) The integrated circuit of Claim 26, wherein each of the input/output block tiles in the column has an identical layout.

28. (Original) The integrated circuit of Claim 26, wherein the integrated circuit is a field programmable gate array.

29. (Original) The integrated circuit of Claim 26, wherein the integrated circuit is disposed on a semiconductor die, the semiconductor die having a first side, a second side opposite the first side, a third side, and a fourth side opposite the third side, and wherein the column of tiles extends from the first side and to the second side, a first input/output block tile of the column being disposed adjacent the first side of the die, a second input/output block tile of the column being disposed adjacent the second side of the die.

30. (Original) An integrated circuit comprising:

a plurality of configurable logic block tiles; and

a plurality of input/output block tiles disposed in columns, each of the columns extending in a first direction, wherein no two input/output block tiles of the integrated circuit are disposed adjacent to one another to form a row that extends in a second direction perpendicular to the first direction.

31. (Original) The integrated circuit of Claim 30, wherein the integrated circuit comprises at least three columns of input/output block tiles.

32. (Original) An integrated circuit consisting essentially of tiles, the integrated circuit comprising:

a input/output block tile having four sides, wherein the input/output block tile is bounded on each of its four sides by another tile.

33. (Original) An integrated circuit comprising:

a plurality of input/output block tiles disposed in a column; and

a plurality of bond bumps, each of the bond bumps being connected to one of the input/output block tiles in a one-to-one relation, wherein some of the bond bumps are disposed outside the column to a first side of the column, and wherein other of the bond bumps are disposed outside the column to a second side of the column opposite the first side.

34. (Original) The integrated circuit of Claim 33, further comprising:

a second plurality of tiles that are not input/output block tiles, wherein the plurality of bond bumps are disposed over the second plurality of tiles.

REMARKS

The above amendments to Claims 2, 4, and 6 were to done correct clerical errors.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicants' attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on September 25, 2003.

Pat Slaback
Name

Signature